In the Claims

Amend the claims as follows:

1. (Currently Amended) A dynamic semiconductor memory device, comprising:

a memory cell array including a plurality of memory cells, the memory cell array being divided into a plurality of blocks;

a block decoder for decoding row address signals and producing block selection signals;

a refresh cycle control circuit, formed on the row decoder, for dividing the block selection signals by preset frequency dividing ratios to set refresh cycles for the blocks, the refresh cycle control circuit having a fuse circuit for setting the frequency dividing ratios and a frequency divider for dividing the block selection signals by frequency dividing ratios set in the fuse circuit; and

a row decoder for selecting the blocks in response to the block selection signals.

2. (Canceled) The dynamic semiconductor memory device according to Claim 1, wherein the refresh cycle control circuit comprises:

a fuse circuit for setting the frequency dividing ratios; and
a frequency divider for dividing the block selection signals by frequency dividing ratios set in the fuse circuit.

3. (Canceled) The dynamic semiconductor memory device according to Claim 2, wherein the fuse circuit is formed on the row decoder.

4-10. (Withdrawn)

11. (Currently Amended) A method of selectively controlling a refresh cycle time of a dynamic semiconductor memory device, comprising:

dividing a memory cell array including a plurality of memory cells into a plurality of blocks;
decoding row address signals and a plurality of producing block selection signals;

dividing the block selection signals by preset frequency dividing ratios to set refresh cycles for the blocks using a refresh cycle control circuit; ~~and~~

selecting the blocks in response to the block selection signals with a row decoder;

setting the frequency dividing ratios with a fuse circuit;

dividing the block selection signals by frequency dividing ratios set in the fuse circuit using a frequency divider; and

forming the fuse circuit on the row decoder.

12. (Canceled) The method according to Claim 11, further comprising:

setting the frequency dividing ratios with a fuse circuit; and
dividing the block selection signals by frequency dividing ratios set in the fuse circuit using a frequency divider.

13. (Canceled) The method according to Claim 12, further comprising forming the fuse circuit on the row decoder.